substrates each comprise a signal core layer, and said third substrate comprises a power core layer.

14. (Amended) The multi-layered circuit structure in accordance with claim 12, wherein said via through holes of said inner power core layer comprise undercut contact surfaces, and said via through holes of each of said signal core layers each have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said power core layer.

REMARKS

Reconsideration of the above-identified patent application is respectfully requested in view of the foregoing amendments and following remarks. The drawings and claims 1, 2, 4 through 7, 11, 12, and 14 have been amended to reduce the ambiguities astutely stated by Examiner Alcala in the present Office Action, in accordance with 35 U.S.C. §112. Claims 1, 2, 4 through 7, 11, 12, and 14 remain in this application.

Attorney for applicant wishes to express regret for any confusion that the former claim language, featuring "spaced-apart" laminate layers, has caused the Examiner. This

Attorney has diligently tried to resolve all the difficulties astutely mentioned by the Examiner.

The invention features a circuit board laminate structure having three-layers, and comprising an inner power core layer 14, that is connected between two signal core layers 12, as shown in the three separate embodiments depicted in exploded views of FIGURES 1, 2, and 3. Upon lamination of the signal layers 12 to the inner core layer 14, the circuit board structure is electrically connected. The laminated circuit board inner power core layer 14 comprises filled via through holes 16 of conductive adhesive. The conductive power core layer vias make contact with the metal pads 3 of conductive vias 15, of the respective outer signal core layers 12.

The rejection of the claims under 35 U.S.C. §102(b) as anticipated by DUFFY et al and 35 U.S.C. §103(a) is respectfully traversed for the following reasons:

The patent to DUFFY teaches the construction of multi-layered sub-modules shown in FIGURES 2a, 2B, and 2C, which eventually form a larger composite modular structure, illustrated in FIGURE 4. All of the multi-layered sub-modules do not have the SIMPLE LAYERS as claimed for the invention. The first and third layers of the invention comprise signal core layers, and the second (inner) layer is a power core

layer. By contrast each of the three-layered structures as comprising the sub-modules of DUFFY et al, comprise a power core 12 surrounded by a dielectric layer 14. These complex layers are then put together to form extended vias, which are metallically coated by conductive layers 16, 18, 32, and 36 to form a multi-layered conductor in the vias, as shown in FIGURES 3A, and 3B. Applicant is doing none of this. The claims of this invention define over the structure of DUFFY et al, and applicant's vias are electrically connected at their pads in the three separate embodiments shown in FIGURES 1, 2, and 3. Furthermore, the middle layer 14 (power core layer of applicant's invention) has vias 16, which are filled in FIGURES 1 and 2, but not in FIGURE 3. By contrast, all of the vias of DUFFY et al are filled throughout all the layers and sub-modules, please see FIGURE 4.

DUFFY et al has an entirely different structure, and different electrically connected vias. DUFFY et al, with all due respect, has no similarity to this invention.

The rejections based on 35 U.S.C. §112 are respectfully traversed, as are the art rejections under 35 U.S.C. §§102 and 103.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

In view of the foregoing amendments and remarks, Applicants respectfully request that claims 1, 2, 4 through 7, 11, 12, and 14 be allowed and that the application be passed to issue.

Respectfully submitted,

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks Washington, D.C. 20231

on 9/9/02 (Date of Deposit)

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9/9/02 (Date)

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 3 and 13 have been canceled. Claims 1, 2, 4 through 7, 11, 12, and 14, have been amended as indicated.

1. (Amended) A [multi] three-layered, laminated circuit structure, comprising:

a first substrate having conductive via through holes disposed therein; [and]

a second substrate laminated to said first substrate and having conductive, adhesive-filled via through holes that align with, and make electrical contact with, the conductive via through holes of said first substrate[upon lamination of said first and second substrates.]; and

a third substrate laminated to said second substrate having via through holes that align with, and make electrical contact with, the adhesive filled via through holes of said second substrate, thus forming said three-layered, laminated circuit structure.

2. (Twice Amended) The [multi] three-layered circuit structure in accordance with claim 1, wherein said first and third [substrate] substrates each comprise [comprises] a signal core layer, and said second substrate comprises a power core layer.

4. (Twice Amended) The [multi] three-layered circuit structure in accordance with claim [3]2, wherein said via through holes of said [inner] power core layer comprises undercut contact surfaces, and said via through holes of each of said [pair of spaced-apart] signal [cores] core layers have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said [inner] power core layer.

5. (Amended) A multi-layered circuit structure, comprising:

a first substrate having conductive via through holes disposed therein; and

a second substrate laminated to said first substrate, and having via through holes comprising conductive adhesive coated pads that align with, and make electrical contact with, the conductive via through holes of said first substrate [upon lamination of said first and second substrates].

6. (Twice Amended) The multi-layered circuit structure in accordance with claim 5, wherein said first substrate comprises a signal core layer, and said second substrate comprises a power core layer.

7. (Amended) The multi-layered circuit structure in accordance with claim 5, [wherein said first] further comprising a third substrate having similar structure to that of said first substrate, said first and third substrates each being laminated to said second substrate, and wherein said first and third substrates each define a signal core layer, [comprises a pair of spaced-apart outer signal cores, and] said second substrate further defining [comprises] an inner power core layer sandwiched between each of said [pair of spaced-apart outer] signal [cores] core layers.

11. (Amended) A multi-layered circuit structure, comprising:

first and second [spaced-apart] substrates, each having conductive via through holes disposed therein; and

a third substrate laminated between said first and second [spaced-apart] substrates and having conductive, adhesive-filled via through holes that align with, and

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make electrical contact with, the conductive via through holes of said first and second [spaced-apart] substrates[, upon lamination of said first and second spaced-apart substrates to said third substrate].

12. (Amended) The multi-layered circuit structure in accordance with claim 11, wherein said first and second [spaced-apart] substrates each comprise a signal core layer, and said third substrate comprises a power core layer.

14. (Amended) The multi-layered circuit structure in accordance with claim [13]12, wherein said via through holes of said inner power core layer comprise undercut contact surfaces, and said via through holes of each of said [spaced-apart outer] signal [cores] core layers each have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said [inner] power core layer.

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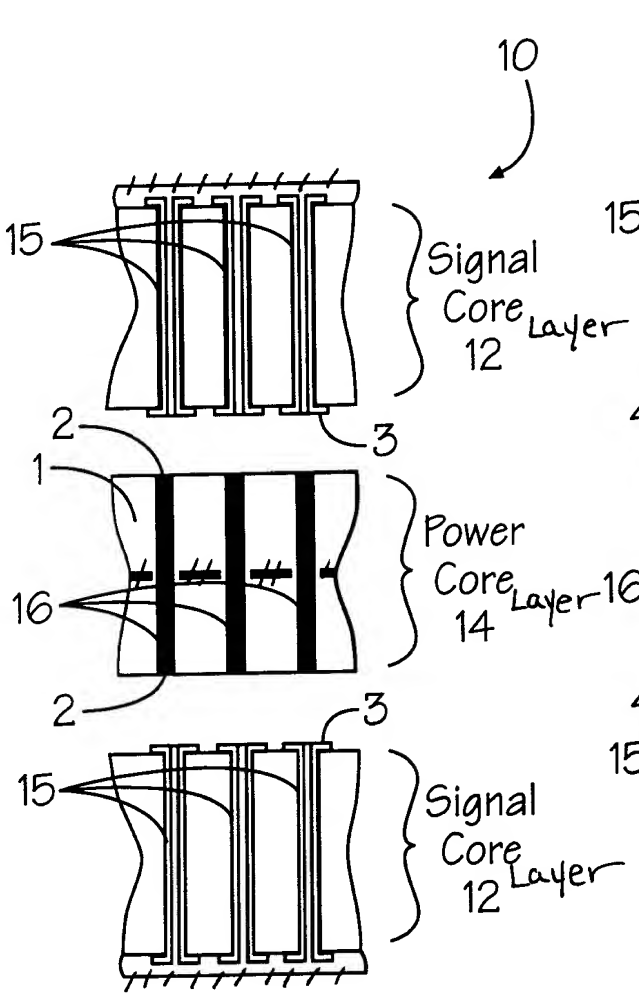

Figure 1

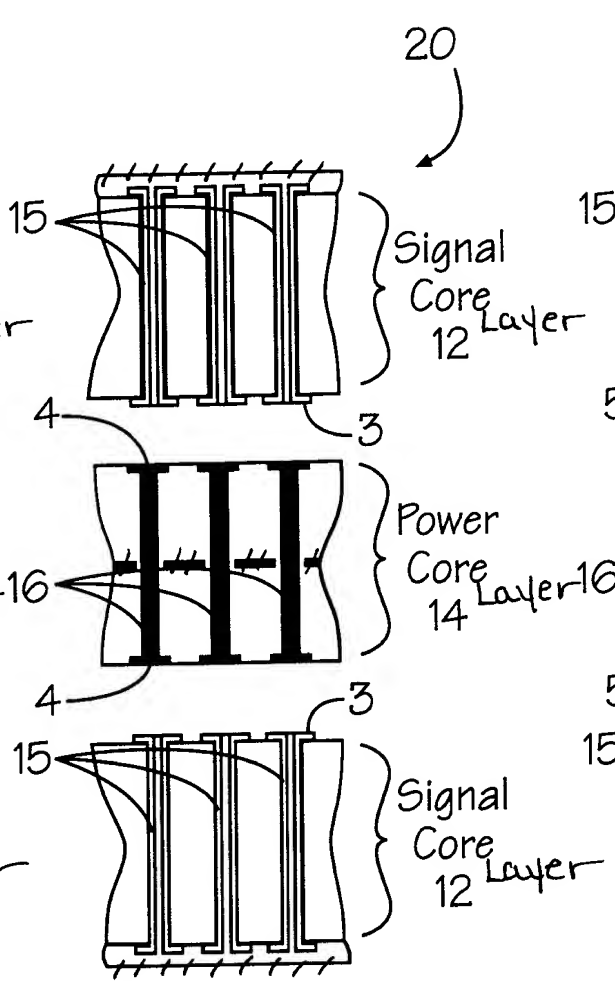

Figure 2

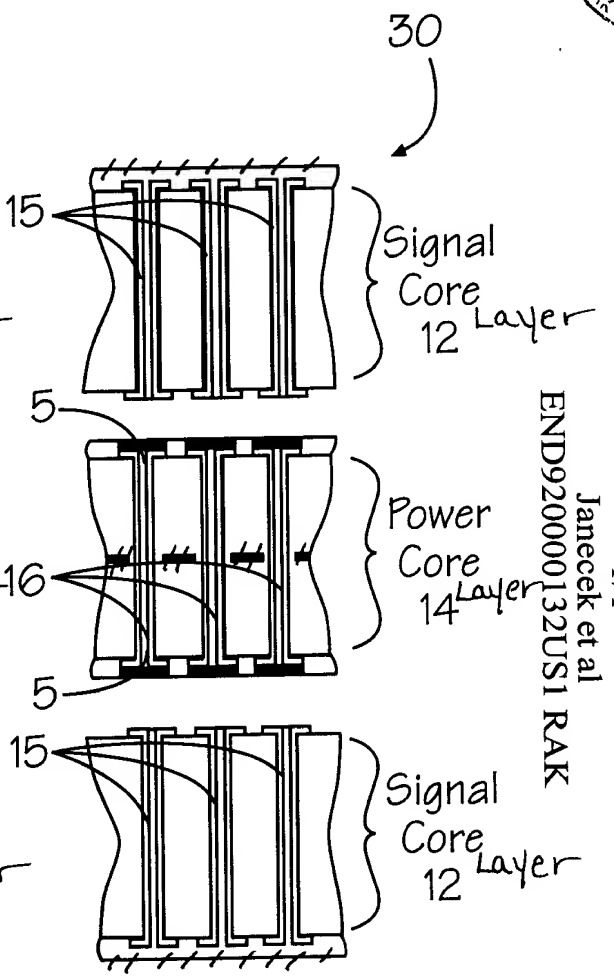

Figure 3

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